

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((reallocate\$3 reprogram\$4 reconfigure\$7) with (partial\$2 portion subset part\$3) with (PLD\$1 pga\$1 FPGA\$1 DFPGA\$1 cpld\$1 prom pla pal/gal (logic adj2 element)) with (logic\$4) ) and ((reallocate\$3 reprogram\$4 reconfigure\$7) with (bitstream bit-stream bit)) and "718"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/07 16:05
L2	6	((reallocate\$3 reprogram\$4 reconfigure\$7) with (partial\$2 portion subset part\$3) with (PLD\$1 pga\$1 FPGA\$1 DFPGA\$1 cpld\$1 prom pla pal/gal (logic adj2 element)) with (logic\$4) with (bitstream bit-stream))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/07 16:06
L3	2	((reallocate\$3 reprogram\$4 reconfigure\$7) with (partial\$2 portion subset part\$3) with (PLD\$1 pga\$1 FPGA\$1 DFPGA\$1 cpld\$1 prom pla pal/gal ) with (logic\$4) with (bitstream bit-stream))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/07 16:09
L4	89	((reallocate\$3 reprogram\$4 reconfigure\$7) with (partial\$2 portion subset part\$3) with (PLD\$1 pga\$1 FPGA\$1 DFPGA\$1 cpld\$1 prom pla pal/gal (logic adj2 element)))) same (bitstream bit-stream)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/07 16:09



[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

Search: ☒ The ACM Digital Library ☐ The Guide



THE ACM DIGITAL LIBRARY

#### Terms used

**reallocate** or **reprogram** or **reconfigure** **near/5** **partial** or **portion** or **subset** or **part** **near/5** **PLD** or **pga** or **FPGA** or **DFPGA** or **cp**

Sort results by

Display results

[Save results to a Binder](#)

[Search Tips](#)

☐ [Open results in a new window](#)

Results 81 - 100 of 200

Result page: [previous](#) [1](#) [2](#) [3](#) [4](#) **5** [6](#) [7](#) [8](#) [9](#) [10](#)

Best 200 shown

#### 81 [Physical design for FPGAs](#)

Rajeev Jayaraman

April 2001

**Proceedings of the 2001 international symposium on Physical design**

Full text available: [pdf\(212.09 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

FPGAs have been growing at a rapid rate in the past few years. Their ever-increasing gate densities and perform discuss the state-of-the-art in FPGA physical design. Compared to physical design in traditional ASICs, FPGAs p design have evolved differently from their ASIC counterparts. Apart from allo ...

**Keywords:** FPGA, physical design, placement, routing

#### 82 [Data and memory optimization techniques for embedded systems](#)

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsber

April 2001

**ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6

Full text available: [pdf\(339.91 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizati subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipat the form of code transoformations. We next cover a broad spectrum of optimizati ...

**Keywords:** DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data c dissipation, register file, size estimation, survey

#### 83 [Managing dynamic reconfiguration overhead in systems-on-a-chip design using reconfigurable datapaths](#)

Z. Huang, S. Malik

March 2001

**Proceedings of the conference on Design, automation and test in Europe**

Full text available: [pdf\(79.99 KB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

#### 84 [Design methodology for PicoRadio networks](#)

J. da Silva, J. Shamberger, M. Ammer, C. Guo, S. Li, R. Shah, T. Tuan, M. Sheets, J. Rabaey, B. Nikolic, A. Sangio

March 2001

**Proceedings of the conference on Design, automation and test in Europe**

Full text available: [pdf\(328.60 KB\)](#)

Additional Information: [full citation](#), [references](#), [index terms](#)

85 A decade of reconfigurable computing: a visionary retrospective

R. Hartenstein

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:  pdf(768.00 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

86 Interconnect prediction for programmable logic devices

Michael Hutton

March 2001

**Proceedings of the 2001 international workshop on System-level interconnect pre**

Full text available:  pdf(268.08 KB)

Additional Information: [full citation](#), [abstract](#), [refe](#)

Classical interconnect prediction would seem to be a perfect fit for the design of programmable logic architecture rough estimates in the early stages of an architecture development. In practice, empirical methods (evaluation architectures. The primary reasons for this gap between theory and practice are th ...

**Keywords:** architecture, interconnect prodiction, programmable logic device, wireability

87 Configuration compression for FPGA-based embedded systems

Andreas Dandalis, Viktor K. Prasanna

February 2001

**Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field prog**

Full text available:  pdf(203.25 KB)

Additional Information: [full citation](#), [abstract](#), [refe](#)

FPGAs are a promising technology for developing high-performance embedded systems. The density and perfori configuration bit-streams has also increased considerably. As a result, the cost-effectiveness of FPGA-based emi configurations. This paper proposes a novel compression technique that reduces the memory requ ...

88 Matching and searching analysis for parallel hardware implementation on FPGAs

Pablo Moisset, Pedro Diniz, Joonseok Park

February 2001

**Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field prog**

Full text available:  pdf(186.03 KB)

Additional Information: [full citation](#), [abstract](#), [refe](#)

Matching and searching computations play an important role in the indexing of data. These computations are ty predicate. Their inherent sequential nature, either because of data dependences but more often because of very parallelization analysis to exploit significant levels parallelism on traditional architecture ...

89 Performance-driven mapping for CPLD architectures

Deming Chen, Jason Cong, Milos D. Ercegovac, Zhijun Huang

February 2001

**Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field prog**

Full text available:  pdf(265.58 KB)

Additional Information: [full citation](#), [abstract](#), [refe](#)

In this paper we present a performance-driven mapping algorithm, PLAMap, for CPLD architectures which consi minimize the depth of the mapped circuit. Meanwhile, we have successfully reduced the area of the mapped circ product terms, slack-time relaxation, and PLA-packing. We compare our PLAMap with a recent ...

**Keywords:** CPLD, FPGA, PLA-style logic cells, delay optimization, technology mapping

90 Evaluation of the streams-C C-to-FPGA compiler: an applications perspective


Jan Frigo, Maya Gokhale, Dominique Lavenier

February 2001

**Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field prog**

Full text available:

Additional Information:

 [pdf\(180.91 KB\)](#)

[full citation](#), [abstract](#), [refs](#)

The Streams-C compiler ([5]) synthesizes hardware circuits for reconfigurable FPGA-based computers from para functions added to a synthesizable subset of C, and supports a communicating process programming model. The communication among the processes transparently to the programmer. For the hardware processes, the compi

**Keywords:** FPGA, FPGA design tools, configurable computing, hardware-software co-design, high-level synthes

91 [A memory coherence technique for online transient error recovery of FPGA configurations](#)

Wei-Je Huang, Edward J. McCluskey

February 2001

**Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field prog**

Full text available:  [pdf\(271.54 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refs](#)

The partial reconfiguration feature of some of the current-generation Field Programmable Gate Arrays (FPGAs) ( an error recovery process can be executed online with minimal interference of user applications. However, beca memory modules for user applications, a memory coherence issue arises such that memory ...

**Keywords:** FPGA, error recovery, fault tolerance, memory coherence

92 [Coarse grain reconfigurable architecture \(embedded tutorial\)](#)

Reiner Hartenstein

January 2001

**Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available:  [pdf\(167.05 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refs](#)



The paper gives a brief survey over a decade of R&D on coarse grain reconfigurable hardware and related comp computing.

93 [Adaptive interfacing with reconfigurable computers](#)

Neil W. Bergmann, Anwar S. Dawood

January 2001

**Australian Computer Science Communications , Proceedings of the 6th Australasi**

Full text available:  [pdf\(792.71 KB\)](#)  [Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [refs](#)



A reconfigurable computer consists of reconfigurable logic circuits added to a conventional processor to give a c application basis. Despite significant research, reconfigurable computers have failed to gain widespread accepta describes the reasons for this failure and argues that the domain of real-time, reactive computer sys ...

94 [Error detection for adaptive computing architectures in spacecraft applications](#)

David Brodrick, Anwar Dawood, Neil Bergmann, Melanie Wark

January 2001

**Australian Computer Science Communications , Proceedings of the 6th Australasi**

Full text available:  [pdf\(803.02 KB\)](#)  [Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [refs](#)

The Australian FedSat satellite will incorporate a payload to validate the use of adaptive computing architectures: spacecraft, but the space environment also represents unique challenges which must be addressed. An importa 4000 device used on FedSat, are vulnerable to a range of radiation induced errors. A system is ...

95 [Processor verification using efficient reductions of the logic of uninterpreted functions to propositional log](#)

Randal E. Bryant, Steven German, Miroslav N. Velev

January 2001

**ACM Transactions on Computational Logic (TOCL)**, Volume 2 Issue 1

Full text available:  [pdf\(319.93 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refs](#)

The logic of Equality with Uninterpreted Functions (EUF) provides a means of abstracting the manipulation of da logic to propositional formulas, we can apply Boolean methods such as ordered Binary Decision Diagrams (BDD: the formulas describing the verification conditions to greatly simplify the ...

**Keywords:** decision procedures, processor verification, uninterpreted functions


- 96 [Session 2A: embedded tutorial: Challenges and opportunities in broadband and wireless communication](#)  
Jan M. Rabaey, Miodrag Potkonjak, Farinaz Koushanfar, Suet Fei Li, Tim Tuan  
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided d**

Full text available:  [pdf\(295.17 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

Communication designs form the fastest growing segment of the semiconductor market. Both network process resources and design efforts. However, further progress is limited by lack of adequate system methodologies an techniques and tools. The first part addresses network processors (NP) that we study from three v ...

- 97 [The benefits and costs of DyC's run-time optimizations](#)  
Brian Grant, Markus Mock, Matthai Philipose, Craig Chambers, Susan J. Eggers  
September 2000 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 22 Iss

Full text available:  [pdf\(1.59 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

DyC selectively dynamically compiles programs during their execution, utilizing the run-time-computed values o dynamic optimizations are preplanned at static compile time in order to reduce their run-time cost; we call this : polyvariant specialization (enabling both single-way and multi ...

**Keywords:** dynamic compilation, specialization

- 98 [High-level library mapping for memories](#)  
Pradip K. Jha, Nikil D. Dutt  
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5


Full text available:  [pdf\(209.38 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

We present high-level library mapping, a technique that synthesizes a source memory module from a library of memories, identify and solve the three subproblems associated with this task, and finally combine these solution intensive designs demonstrate that our memory mapping approach generates a wide variety ...

**Keywords:** high-level synthesis, memory libraries, technology-mapping

- 99 [An autostereoscopic display](#)  
Ken Perlin, Salvatore Paxia, Joel S. Kollin  
July 2000 **Proceedings of the 27th annual conference on Computer graphics and interactive**

Full text available:  [pdf\(16.56 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

We present a display device which solves a long-standing problem: to give a true stereoscopic view of simulatec freely change position and head rotation. Based on a novel combination of temporal and spatial multiplexing, th without requiring the use of special eyewear. The availability of this t ...

**Keywords:** graphics hardware, hardware systems, object tracking, optics, user interface hardware, virtual reali

- 100 [System design of active basestations based on dynamically reconfigurable hardware](#)  
Athanassios Boulis, Mani B. Srivastava  
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available:  [pdf\(111.85 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refe](#)

Providing multiple modes to support dynamically changing environments, standards, and new services is preval contains time-constrained tasks, it is important to analyze the temporal requirements as well as the functional c